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| Notice of Allowability | Application No. 10/783,462 | Applicant(s) FILIPPI ET AL. | |
|---|---|---|---|
| | Examiner Steven J. Fulk | Art Unit 2891 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed June 5, 2006*.

2. ☒ The allowed claim(s) is/are *1-16*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20060525;20060526* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

BRADLEY K. SMITH
PRIMARY EXAMINER

## DETAILED ACTION

## EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Jim Bitetto on June 12, 2006.

The application has been amended as follows:

On page 18, line 7 of the specification, replace --Dummy stacked vias 305 are not-- with --Dummy stacked vias are not--.

On page 18, line 10 of the specification, replace --dummy structure 305 end-- with --dummy structure end--.

### *Response to Arguments*

2. Applicant's amendment filed June 5, 2006, which amends claims 1 and 9 and cancels claims 32-35, has been entered. Claims 1-16 are currently pending.

3. Applicant's arguments, see pages 6-7, with respect to the rejection of claims 1-3, 6, 9-11 and 14 under 35 U.S.C. 102(b) have been fully considered and are persuasive. The rejection of claims 1-3, 6, 9-11 and 14 has been withdrawn.

4. Applicant's arguments, see page 7, with respect to the rejection of claims 4-5, 7-8, 12-13 and 15-16 under 35 U.S.C. 103(a) have been fully considered and are persuasive. The rejection of claims 4-5, 7-8, 12-13 and 15-16 has been withdrawn.

***Allowable Subject Matter***

5. Claims 1-16 are allowed.

6. The following is an examiner's statement of reasons for allowance: a reasonable search of the prior art did not find a method for evaluating reliability of a semiconductor chip comprising building a test structure in accordance with a manufacturing process used in fabricating a semiconductor chip structure to test reliability of the semiconductor chip structure; building the test structure including building a via chain through layers of the semiconductor chip structure such that a plurality of widths of vias are used to adjust strain in different layers, or building a dummy structure to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent structures of the test structure; and thermal cycling the test structure provided by the manufacturing process, as recited by independent claims 1 and 9.

JEDEC Publication JEP139 (PTO-892, Page 1, NPL Reference "U", all NPL references previously provided) discloses a method for evaluating reliability of a semiconductor chip comprising building a test structure in accordance with a manufacturing process used in fabricating a semiconductor chip structure to test reliability of the semiconductor chip structure, but the reference does not teach building the test structure to include building a via chain through layers of the semiconductor chip structure such that a plurality of widths of vias are used to adjust strain in different layers, or building a dummy structure to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent

structures of the test structure; and the thermal cycling is performed by sampling a number of wafers in a test oven, not provided by the manufacturing process.

Suzuki et al. (PTO-892, Page 1, NPL Reference "V") discloses a method of evaluating stress induced failure in Copper dual damascene interconnects by varying via diameter, but the reference does not teach the use of dummy structures to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent structures of the test structure; and the thermal cycling is performed by sampling a number of wafers in a test oven, not provided by the manufacturing process.

Huston et al. (PTO-892, Page 1, NPL Reference "W") discloses a method of detecting reliability defects in semiconductor chips, but the reference does not teach building a via chain through layers of the semiconductor chip structure such that a plurality of widths of vias are used to adjust strain in different layers, or building a dummy structure to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent structures of the test structure. The reference also does not teach thermal cycling the test structures.

Yao et al. '701 teaches a via chain test structure used for stress-induced void reliability monitoring, wherein the test structure includes a dummy structure to provide a via density in an area of the semiconductor chip structure, but the reference does not teach building the test structure to include building a via chain through layers of the semiconductor chip structure such that a plurality of widths of vias are used to adjust strain in different layers; and the thermal cycling is

performed by sampling a number of wafers in a test oven, not provided by the manufacturing process.

Ryan '587 discloses a method of evaluating the thermal stress migration reliability of a semiconductor chip, and teaches that stress migration is the mass transport of interconnect material in response to mechanical stress gradients present in the interconnect which result from thermal expansion coefficient mismatches between the metal layers and surrounding dielectric layers. Fetterman et al. '465, Wang '383 and Werner et al. '901 disclose a Cu dual-damascene test structure with a barrier layer within a semiconductor wafer and method for evaluating stress-induced voids using the test structure, wherein thermal stress is applied and the via resistance shift due to void formation and/or delamination is measured. The references do not teach building a via chain through layers of the semiconductor chip structure such that a plurality of widths of vias are used to adjust strain in different layers, or building a dummy structure to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent structures of the test structure; and the thermal cycling is performed by sampling a number of wafers in a test oven, not provided by the manufacturing process.

Langer et al. '786 discloses a Cu dual-damascene test structure with a barrier layer within a semiconductor wafer and method for evaluating stress-induced voids using the test structure, wherein thermal stress is applied and voids are detected with the use of an electron microscope. Graas et al. '181 discloses a via chain test structure within a semiconductor wafer used evaluating stress-induced voids caused by thermal cycling. Chao et al. '350 discloses a method of performing a thermal

stress cycle test on a semiconductor chip, and the reference teaches that thermal expansion coefficient mismatch between metals and dielectrics causes metal voiding and film peeling during thermal cycles. The references do not teach building a via chain through layers of the semiconductor chip structure such that a plurality of widths of vias are used to adjust strain in different layers, or building a dummy structure to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent structures of the test structure; and the thermal cycling is performed by sampling a number of wafers in a test oven, not provided by the manufacturing process.

Nawa et al. (PTO-892, Page 1, NPL Reference "X") discloses a reliability study for coefficient of thermal expansion mismatching in a semiconductor chip via structure, wherein thermal cycling caused cracks in the interconnects discloses. Ogawa et al. (PTO-892, Page 2, NPL Reference "U") discloses a study of stress-induced voiding in Cu dual-damascene vias with a barrier layer, wherein thermal cycles caused interconnect void failures due to mismatches in thermal expansion coefficients of Cu and the surrounding dielectric. Graas et al. (PTO-892, Page 2, NPL Reference "V") discloses a correlation between via test structure resistance and product reliability, wherein early life failure rate models are used to predict product reliability. Hansen (PTO-892, Page 2, NPL Reference "W") and Papp et al. (PTO-892, Page 2, NPL Reference "X") disclose methods of performing product reliability monitoring based on wafer-level test structures that are manufactured on the same wafer as product chips. The references do not teach building a via chain through layers of the semiconductor chip structure such that a plurality of widths of vias are

used to adjust strain in different layers, or building a dummy structure to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent structures of the test structure; and the thermal cycling is performed by sampling a number of wafers in a test oven, not provided by the manufacturing process.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven J. Fulk
Patent Examiner
Art Unit 2891

June 12, 2006

BRADLEY K. SMITH
PRIMARY EXAMINER